A
3-Days Workshop
On
“Digital and Analog VLSI Design”

Event Date-

10th Aug to 12th Aug. 2017

Event Venue-

Room No.411 4th Floor IOE Building

The Electronics & Telecommunication Engineering Department of Mumbai Education Trust’s, Bhujbal Knowledge City, Institute of Engineering arranged 3-days workshop on “Digital and Analog VLSI Design” for Faculty members (External and Internal), Post Graduate Students from Engineering Colleges.

Aim-

To motivate and aware research areas for the faculty members and PG Students in the field of Digital and Analog VLSI Design.

Course Objective-

VLSI Design is considered as an important domain in the field of Digital and Analog circuits. The main objective of this workshop is to impart through technical knowledge on VLSI design to the faculty and post graduate students towards the research in the field of VLSI.

Program Committee-

Patron

Hon. Dr. Shefali Bhujbal

Advisor

Prof. Dr. V. P. Wani, Principal
MET's Institute of Engineering

Convener

Prof. Dr. V. J. Gond, HOD E&TC
Prof. R. B. Rehpade, HOD Electronics

Organizer

Prof. P. N. Metange, Asst. Professor
Prof. N. L. Ahire, Asst. Professor
Prof. S. M. Dhekane, Asst. Professor
Prof. K.T. Ugale, Asst. Professor

Contact Person-

Mr. R. S. Magaji, Cell:-9503858338
Mr. V. S. Choudhari, Cell: 8806811188E-mail-
metetc.fdp@gmail.com

Event Leaflet-

Registration Form

MET's Institute of Engineering, Adgaon, Nashik
Department of E & TC Engineering
Organizes
A
3 Days workshop on "Digital & Analog VLSI Design"
(10th to 12th Aug 2017)
(Submit the filled registration form to Mr. R. S. Magaji up to 8th August, 2017)

1. Name:
2. College:
3. Mobile Number:
4. Email ID:
5. Payment Details:

Date: _____
Place: _____
Participant Signature

Google Link:-
https://docs.google.com/forms/d/e/1FAIpQLSeAfkyV7z7Oocg3p_tPnDPOMVfuFx3mq6OqCDohy_Q3ngKFkQ/viewform?usp=sf_link

Online Payment Details
Account No- 084100100001278
IFSC Code- SRCB0000084
MICR No- 422088002
Bank Name- The Saraswat Co-op Bank Ltd.
Branch Name - Suyojit Trade Centre Rajiv Gandhi Bhavan, Nasik
Branch Code- 84

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MET Bhujbal Knowledge City

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3 Days
Workshop on
"Digital & Analog VLSI Design"
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Organize by

MET

Department of E & TC Engineering

Bhujbal Knowledge City
Mumbai Education Trust's
Institute of Engineering, Adgaon,
Nashik-422003.

About Institute

Institute Of Engineering was established in 2006 at BKC under the umbrella of MET with world class infrastructure, centralized library, conference rooms, seminar halls, and amphitheatre. IOE was fully dedicated and well qualified faculty with passion who consider teaching as mission rather than profession.

About Department

The Electronics & Telecommunication Engineering Department of Mumbai Education Trust's, Bhujbal Knowledge City, Institute of Engineering was established in the year 2006, and has grown over the years into a competent department with state of the art computing facilities, and dedicated faculty. Having started with a four year under-graduate program, B.E (Electronics & Telecommunication).
The department emphasizes the vision of the Mumbai Education Trust's, Bhujbal Knowledge City (MET-BKC) for excellence in education. Highly qualified, dedicated faculty and good infra-structure facilities, make this dream realizable.

Course Objective

VLSI Design is considered as an important domain in the field of Digital and Analog circuits. The aim of this workshop is to impart through technical knowledge on VLSI design to the faculty and students towards the research in the field of VLSI.

Who can attend?

The workshop is open to the faculty members and PG Students who want to make career in VLSI Design

Registration Fees

Rs.1200/- Per Participant
(Including Lunch & Breakfast)
Accommodation Charges Extra

Course Materials

CD containing required software and materials.

Important dates

Last Date of Acceptance of registration form 8th August, 2017

Note

Only 40 candidates will be selected on first come first serve basis.

Program Content

Note:-Program will start sharp at 9.30 am.

Day1
Introduction to Analog design
VLSI Research Areas

Day2
FPGA Design Flow
FPGA implementation of Real time Case Study

Day3
Digital CMOS Circuit design using dsch
Digital CMOS Layout design in Microwind
Different ways to implement Digital design using Xilinx

Program Outcome

The workshop will help to improve the knowledge in VLSI Design and one step move towards in the area of researches in VLSI.

Resource Person

Prof. Dr. S. P. Ugale, KKWIEER, Nashik
Prof. M.P.Mahajan. SITRC, Nashik
Prof. Dr. Sanjeev Sharma, SITRC, Nasik
Prof. Dr. S.D. Pable,
Govt. Polytechnic, Nasik

Day 1 Schedule

Time	Activity
10:00am- 10:20am	Registration
10:20am-10:40am	Tea & Snacks
10:40am-10-50am	Welcome & Inaugural Function
10:50am-11:00am	Key note address by Principal Sir
Resource Person : **Prof. Dr. S. P. Ugale** **KKWIEER, Nasik**	
11:00am-11:30am	Basics of CMOS Circuit Design
11:30am12:00am	Combinational Circuits Design using CMOS
12:00am-12:30pm	Design Rules
12:30pm-1:00pm	Digital CMOS Circuit design using dsch
1:00pm-1:40pm	Lunch Break
1:45pm-3:00pm	Digital CMOS Layout design in Micro wind
3:00pm-3:10pm	Tea Break
3:10pm-4:30pm	Different ways to implement Digital design using Xilinx

Day 1 activity

Prof. Sandeep Dhekane Welcome to Hon. Chief Guest Prof. Dr. Sunita P. Ugale madam, Respected Principal Prof. Dr. V. P. Wani sir, Prof. Dr. V. J. Gond sir(HOD E&TC), Prof. R.B. Rehpade Sir (HOD Electronics), and Prof. D. B. Ahire Sir on the occasion of inaugural function of “Digital and analog VLSI Design” workshop. He has given a brief introduction about the resource person.

Respected Principal Prof. Dr. V. P. Wani sir felicitate Resource Person Hon. Chief Guest Prof. Dr. Sunita P. Ugale madam from KKWIEER, Nasik.

Madam has published more than 50 papers in the field of VLSI and also teaching experience more than 20+ years.

Our honorable Principal Prof. Dr. V. P. Wani sir addressed to the participants and gives guidance about workshop.

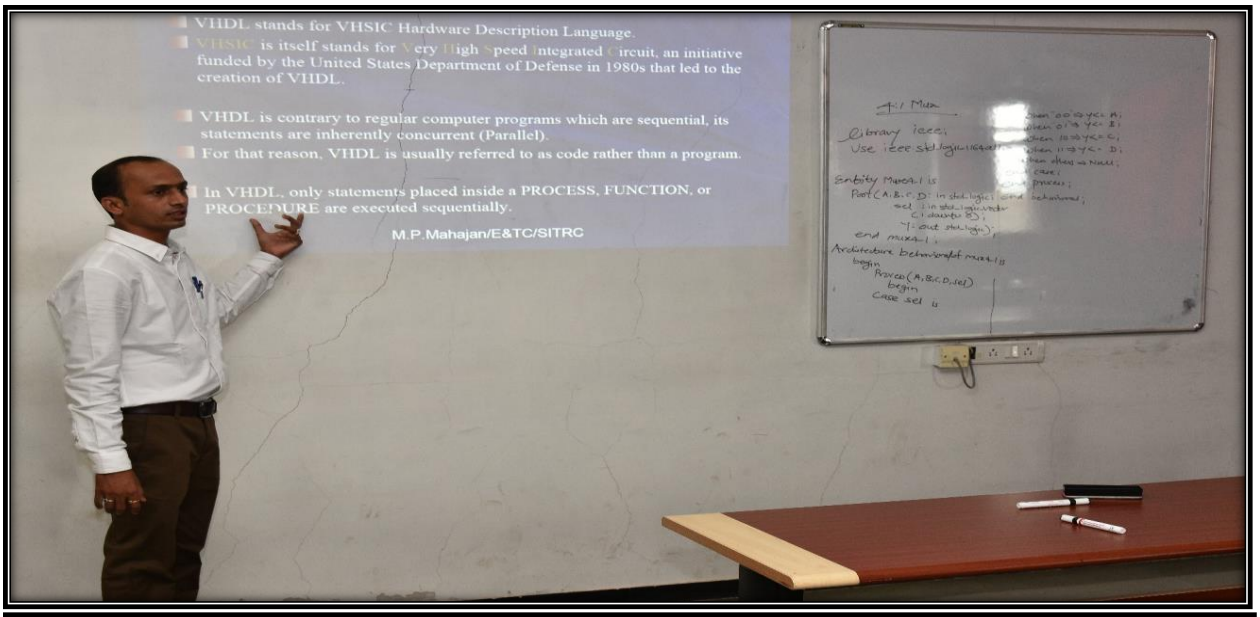
Prof. Dr. Sunita P. Ugale madam has been discussed on the basics of CMOS Circuit Design, Combinational Circuits Design using CMOS, Design Rules, and digital CMOS Circuit design using dsch, Digital CMOS Layout design in Micro wind, and hands on practice for 2 hours to the participants on the different ways to implement Digital design using Xilinx

Day 2 Schedule

Day 2 Date:11-08-17	
10:20am-10:40am	Tea & Snacks
10:40am-12:00am	Different Modeling Styles
12:00am-1:00pm	Introduction to FPGA Design Flow
1:00pm-1:40pm	Lunch Break
1:45pm-2:30pm	Combinational & Sequential Circuits
2:30pm-3:00pm	Verification of Design using Test bench
3:00pm-3:10pm	Tea Break
3:10pm-3:40pm	FSM Designing
3:40pm-4:40pm	Practical Session

Day 2 activity

Respected HOD of Electronics department Prof. R.B. Rehpade Sir felicitate Resource Person Hon. Chief Guest Prof. Mukesh P. Mahajan from SITRC, Nasik. Sir has 7+Years of experience in field of VLSI and number of papers published in national and international Journals.



Prof. Mukesh P. Mahajan sir has been discussed theory session on different Modeling Styles, introduction to FPGA Design Flow, Combinational & Sequential Circuits and verification of design using Test bench.

Prof. Mukesh P. Mahajan sir has been taken Practical session and explain how to write the VHDL code in Xilinx 9.1, how to execute the code, and make bit file to download on FPGA and verify the functionality.

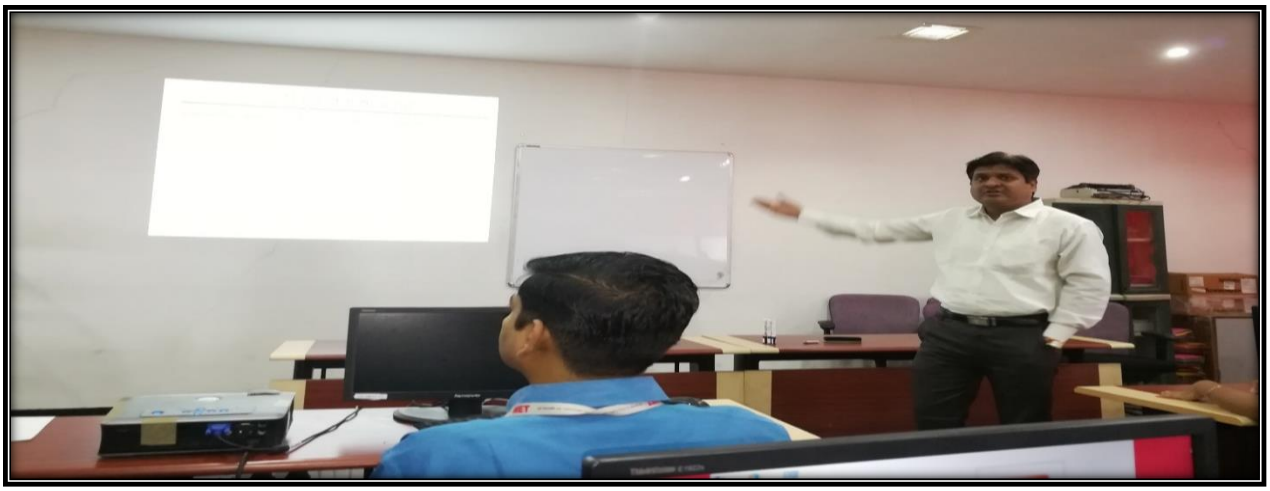
Day 3 Schedule

Day 3 Date:12-08-17	
9:45am-10:00am	Felicitation
10:00am-12:00am	VLSI Design Issues and Solutions
12:00am-12:10pm	Tea & Snacks
12:15am-2:15pm	Design of an Optimized Processor and Partitioning using KL Algorithm
2:15pm-2:50pm	Lunch Break
2:50pm-3:20pm	Valedictory Function
3:20pm-3:40pm	Feedback form Distribution & collection
3:40pm-4:00pm	Certificate & CD Distribution

Day 3 activity

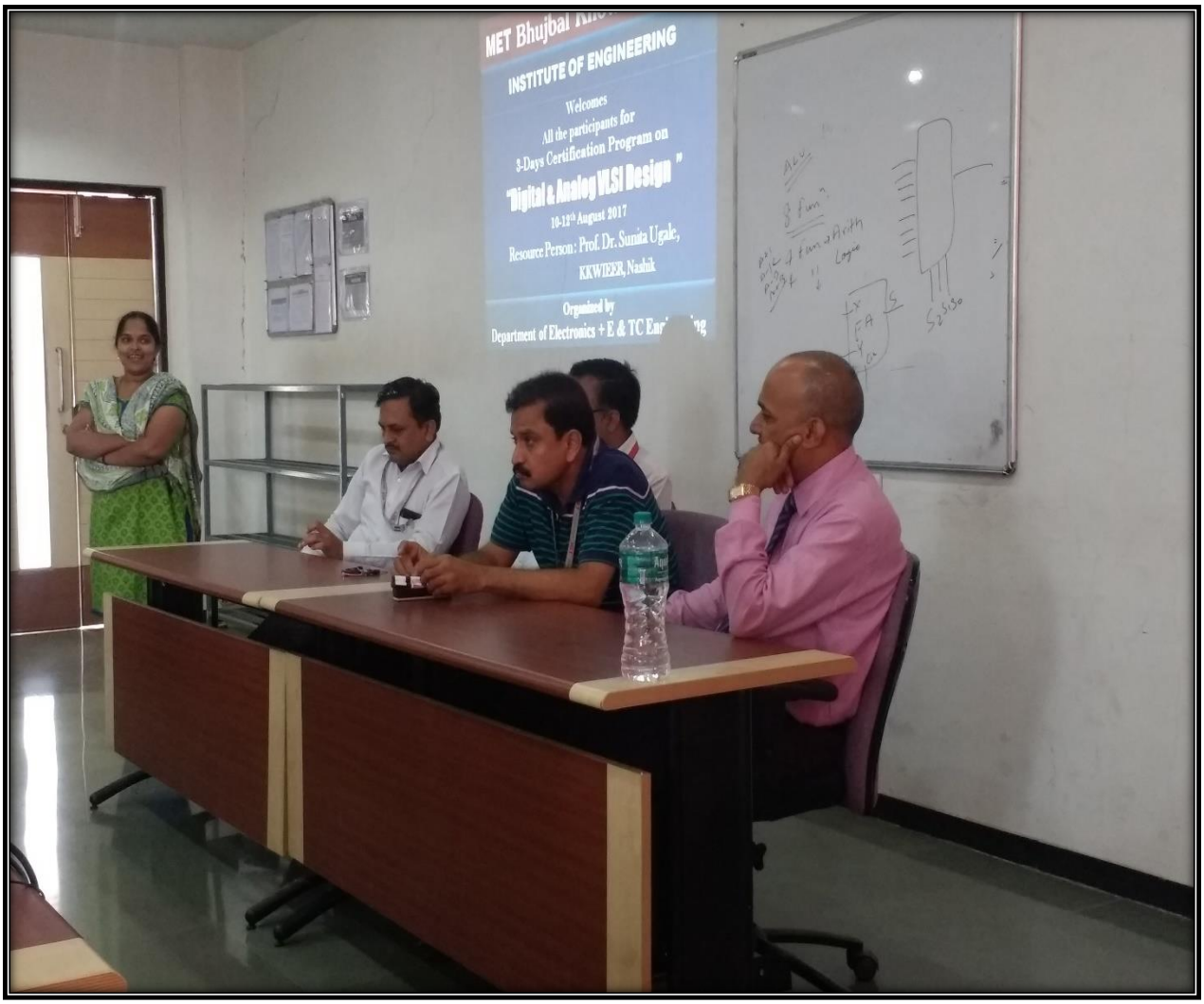
Prof. Sandeep Dhekane Welcome to Hon. Chief Guest Prof. Dr. Sachin D. Pable sir and gives his brief introduction. Sir has published number of national and international journal papers. Sir has more than 20+ years of teaching experience and also work in the research area of VLSI.

Respected HOD of E&TC department Prof. Dr. V. J. Gond Sir felicitate Resource Person Hon. Chief Guest Prof. Dr. Sachin D. Pable from Government polytechnic, Nasik



Prof. Dr. Sachin D. Pable sir has been discussed theory session on VLSI Design Issues and Solutions.

Prof. Dr. Sanjeev Sharma sir has been discussed theory session on design of an Optimized Processor and Partitioning using KL Algorithm.



Participants from KKWIEER Nasik Prof. K Nirmala kumari gives her feedback about 3-days workshop. She has tell about before coming to the session only HOD has forcing them to attend the workshop so because of that she was attending it but after attending the session she has appreciating the Dr. Sharma sir lecture related to research topic and challenges in fields of VLSI

Participants from PG Students Miss Ashwinee D. Jadhao gives her feedback about 3-days workshop. She has tell us about hands on experience which was conducted by Prof Ugale madam and Prof Mahajan Sir and also she has very happy to get some new topic in VLSI for her Masters project from Dr. Pable Sir.

Certificate Distribution

1] Participants Prof. Priyanka Kulkarni from Late. G. N. Sapkal COE Nasik receiving Certificate from Dr. V. J. Gond.

2] Participants Prof. Anni Gupta receiving Certificate from D. B. Ahire.

3] Participants Prof. Shailendra Vidhate receiving Certificate from Prof. R. B. Rehpade.

4] Participants Prof. Savita Deore receiving Certificate from Dr. Sanjeev Sharma

Vote of Thanks

Prof. P. N. Metange propose vote of thanks and official announcement of program end.

Program Outcome

The workshop will help to improve the knowledge in VLSI Design and one step move towards in the area of researches in VLSI.